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10/849,958	05/21/2004	Hitoshi Takahashi	19546.0067	8037

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EXAMINER	
NAM, HYUN	

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2184	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

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Office Action Summary	Application No.	Applicant(s)	
	10/849,958	TAKAHASHI, HITOSHI	
	Examiner	Art Unit	
	Hyun Nam	2184	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 October 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) *17-20* is/are withdrawn from consideration.

5)☒ Claim(s) *13 and 16* is/are allowed.

6)☒ Claim(s) *1-3, 6-8, 9, 11, and 21* is/are rejected.

7)☒ Claim(s) *4, 5,10, 14 and 15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/ are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections - Formality

Claims 1, 2, 6, 7, 9, 11-13, 16 and 21 are objected to because of the following informalities:

The following is a quotation of 37 CFR § 1.75(i):

> (i.) Where a claim sets forth a plurality of elements or steps, each element or step of the claim should be separated by a line indentation.

Claims 1, 2, 6, 7, 9, 11-13, 16 and 21 objected to for containing a plurality of elements or steps which are not separated by a line indent. An amendment is required to put the claim in proper format. Line indents aid in understanding the logical grouping of a claim's elements.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3, 6-9, 11-12, and 21 are rejected under 35 U.S.C. 102(b) as anticipated by Muller (U.S. Patent 4,807,141), hereinafter Muller '141.

Referring to claim 1, Muller '141 teaches, as claimed, a microcomputer, resettable by a reset signal from outside, for performing processes under control of a control program, the microcomputer comprising:

an input and output circuit (computer means, see Column 2, Line 52) having a plurality of operation modes (processing operating data and protecting operating data, see Column 2, Lines 55-57);

a control signal generator (computer means) for generating a write signal in an operation mode setting routine of the control program (transfer operating data from the microprocessor to the non-volatile memory, see Column 3, Lines 9-11);

a control circuit (microprocessor, see Column 3, Line 5) for setting the operation mode of the input (input signals, see Column 3, Line 9) and output circuit in response to the write signal (transfer operating data from the microprocessor to the non-volatile memory, see Column 3, Lines 9-11); and

a protection circuit (third switching means, see Column 3, Lines 16-26) for protecting the input and output circuit from being reset in operation mode from receiving a first signal of the write signal to receiving the reset signal the protection circuit is reset by the reset signal from the outside once the control circuit has set the operation mode by receiving the first signal of the write signal (see Column 3, Line 16-26),

wherein the input and output circuit receives a signal from and sends a signal to the outside in accordance with the operation mode set by the control circuit (see Column 3, Lines 16-26; Note, the inhibition of power down signal from second switching means is not processed until microprocessor has transferred the operating data).

Referring to claim 2, Muller '141 teaches, as claimed, an operation mode control circuit in a microcomputer, resettable by a reset signal from the outside, for performing processes under the control of a control program, the operation mode control circuit comprising:

a control signal generator circuit (see Fig. 3c) for generating a first output signal, being output during a first subsequence for a reset (reset, see Column 12, Line 1-3) of the microcomputer and for generating a second output signal (write

signal, see Fig. 3b, WR) for setting an operation mode of an input and output circuit (Note, sets the operation mode to 'write to NVM');

a write protection circuit (third switching means, see Column 3, Lines 16-26) for generating a buffer signal (including buffer means, see Column 3, Line 12) in response to a first signal of the first output signal; and

a control circuit for latching the second output signal (write enable, see Fig. 3b, WE) from the control signal generator in response to the buffer signal from the write protection circuit,

wherein the control circuit sets an operation mode of an input and output circuit, which receives a signal from and sends a signal to the outside, in accordance with the latched second output signal (see Column 3, Lines 16-26; Note, the inhibition of power down signal from second switching means is not processed until microprocessor has transferred the operating data)..

As to claim 3, Muller '141 teaches an operation mode control circuit as claimed in claim 2, wherein the first output signal comprises a pulse signal (see Fig. 3c, RST).

Referring to claim 6, Muller '141 teaches, as claimed, a microcomputer, comprising:

an operation mode control circuit (computer means, see Column 2, Line 52), wherein the operation mode control circuit includes a control signal generator (see Fig. 3c), for generating a first output signal, being output during a first subsequence for a reset (reset, see Column 12, Line 1-3) of the microcomputer and for generating a second output signal (write signal, see Fig. 3b, WR) for setting an operation mode of an input and output circuit (Note, sets the operation mode to 'write to NVM'), a write protection circuit (third switching means, see Column 3, Lines 16-26) for generating a buffer signal (including buffer means, see Column 3, Line 12) in response to only a first output signal the control signal generator outputs first subsequent to the reset of the microcomputer, and a control circuit for latching a second output signal from the control signal generator in response to the buffer signal from the write protection circuit (see Column 3, Lines 16-26; Note, the inhibition of power down signal from second switching means is not processed until microprocessor has transferred the operating data);

an input and output circuit (computer means, see Column 2, Line 52) for receiving a signal from and sending a signal to the outside; and

a data register (see Fig. 2, Registers) for latching a data signal from the operation mode control circuit in response to a data register write signal from the operation mode control circuit (see Fig. 2),

wherein the data register outputs, to the input and output circuit, a signal responsive to the data signal (see Fig. 2).

Referring to claim 7, Muller '141 teaches, as claimed, an operation mode control circuit in a microcomputer for performing processes under the control of a control program, the operation mode control circuit comprising:

a control signal generator (see Fig. 3c) for generating a first output signal output during a first subsequence for a reset for microcomputer (reset, see Column 12, Line 1-3), for generating a second output signal (write signal, see Fig. 3b, WR) for setting an operation mode (Note, sets the operation mode to 'write to NVM') of an input and output circuit and for generating a first decode signal and a second decode signal (see Fig. 2; Note, in a binary system such as the computer, +5VDC has been decoded to mean logic 1 and 0VDC has been decode to mean logic 0);

a write protection circuit (third switching means, see Column 3, Lines 16-26) for generating a buffer signal (including buffer means, see Column 3, Line 12) that is a buffered version of the first output signal from the control signal generator only if the first decode signal having predetermined data and the second decode signal having predetermined data have been successively received from the

control signal generator (see Fig. 3b, AND Gate 654; Note, WE is latched when WR and RST/658A is True); and

a control circuit (microprocessor, see Column 3, Line 5) for latching a second signal from the control signal generator in response to the buffer signal from the write protection circuit (write enable, see Fig. 3b, WE),

wherein the control circuit-sets, in response to the second output signal latched, the operation mode of an input and output control circuit that receives a signal from and sends a signal to the outside (see Column 3, Lines 16-26; Note, the inhibition of power down signal from second switching means is not processed until microprocessor has transferred the operating data).

Referring to claim 8, Muller '141 teaches, as claimed, an operation mode control circuit as claimed in claim 7, wherein the first output signal comprises a pulse signal (see Fig. 3c, RST).

Referring to claim 9, Muller '141 teaches, as claimed, an operation mode control circuit in a microcomputer, resettable by a reset signal from the outside, for performing processes under the control of a control program, the operation mode control circuit comprising:

a control signal generator (see Fig. 3c) for generating a first output signal output during a first subsequence for a reset (reset, see Column 12, Line 1-3) for microcomputer, for generating a second output signal (write signal, see Fig. 3b, WR) for setting an operation mode (Note, sets the operation mode to 'write to NVM') of an input and output circuit and for generating a plurality of decode signals (see Fig. 2; Note, in a binary system such as the computer, +5 VDC has been decoded to mean logic 1 and 0 VDC has been decode to mean logic 0);

a write protection circuit (third switching means, see Column 3, Lines 16-26) for generating a buffer signal (including buffer means, see Column 3, Line 12) that is a buffered version of the first output signal from the control signal generator only if the plurality of decode signals having predetermined data have been successively received from the control signal generator (Note, only certain sequence of decoded logic will make this machine work); and

a control circuit (microprocessor, see Column 3, Line 5) for latching a second signal from the control signal generator in response to the buffer signal from the write protection circuit (write enable, see Fig. 3b, WE),

wherein the control circuit sets, in response to the second output signal latched, the operation mode of an input and output control circuit that receives a signal from and sends a signal to the outside (see Column 3, Lines 16-26; Note, the

inhibition of power down signal from second switching means is not processed until microprocessor has transferred the operating data).

Referring to claim 11, Muller '141 teaches, as claimed, a microcomputer comprising:

an operation mode control circuit (computer means, see Column 2, Line 52), wherein the operation mode control circuit includes a control signal generator (see Fig. 3c) for generating a first output signal output during a first subsequence for a reset (reset, see Column 12, Line 1-3) for microcomputer, for generating a second output signal (write signal, see Fig. 3b, WR) for setting an operation mode of an input and output circuit and for generating a first decode signal and a second decode signal (see Fig. 2; Note, in a binary system such as the computer, +5 VDC has been decoded to mean logic 1 and 0 VDC has been decode to mean logic 0), a write protection circuit (third switching means, see Column 3, Lines 16-26) for generating a buffer signal (including buffer means, see Column 3, Line 12) that is a buffered version of the first output signal from the control signal generator only if a first decode signal having predetermined data and a second decode signal have been received from the control signal generator, and a control circuit for latching a second signal from the control signal generator in response to the buffer signal from the write protection circuit (Note, only certain sequence of decoded logic will make this machine work);

an input and output control circuit (computer means, see Column 2, Line 52) for controlling signal inputting from and signal outputting to the outside; and

a data register (see Fig. 2, Registers) for latching a data signal from the operation mode control circuit in response to a data register write signal from the operation mode control circuit (see Fig. 2),

wherein the data register outputs a signal responsive to the data signal to the input and output control circuit (see Fig. 2).

Referring to claim 12, Muller '141 teaches, as claimed, a operation mode control circuit in a microcomputer for performing processes under the control of a control program, the operation mode control circuit comprising:

a control signal generator (see Fig. 3c);

a write protection circuit (third switching means, see Column 3, Lines 16-26) for latching a second output signal from the control signal generator in response to a first output signal from the control signal generator, and for generating a write signal (write signal, see Fig. 3b, WR) responsive to the logical value of the second output signal latched in the write protection circuit (write enable, see Fig. 3b, WE); and

a control circuit (computer means, see Column 2, Line 52) for latching third output signal from the control signal generator in response to the write signal and for generating a control signal responsive to a logical value of the third output signal latched in the control circuit,

wherein the write signal is a signal with a fixed logical value if the logical value of the second output signal latched in the write protection circuit is "0", the write signal is a buffer signal that is the buffered version of the first output signal from the control signal generator if a logical value of the second output signal latched in the write protection circuit is "1" (see Fig. 3b. Inverter 654B; Note, WR signal is inverted from "0" to "1" or "1" to "0"), and

the control signal is supplied to a selection circuit (see Fig. 3c, RST and PWR) that selects one signal generator from among a plurality of signal generators, each containing at least a data register (see Fig. 3b, Note, each gate registers data), for sending a signal to the outside.

Claim 21 is rejected under 35 U.S.C. 102(b) as being anticipated by Wakasugi (U.S. Patent Number 4,228,502) hereinafter Wakasugi '502.

Referring to claim 21, Wakasugi '502 teaches, as claimed, a control system comprising:

a microcomputer (see Fig. 2), wherein the microcomputer includes an input and output circuit (see Fig. 2 Keyboard 6 and Floppy Disk Unit 7) having a plurality of operation modes (see Fig. 2; Note, computer have plurality of operation modes), a control signal generator (see Fig. 2) for generating a write signal (see Fig. 2) in an operation mode setting routine of the control program (see Column 3, Lines 34-37), a control circuit for setting an operation mode of the input and output circuit in response to the write signal (see Column 4, Lines 13-15), and a protection circuit for protecting the input and output circuit from being reset in operation mode until the protection circuit is reset by a reset signal from the outside once the control circuit has set the operation mode (see Column 3, Lines 17-24), a monitoring signal output port (see Fig. 4, timer 43 output) for outputting a monitoring signal to the watchdog timer (see Fig. 4, timer 43) , a reset signal input port (see Fig. 4, timer 43 input) for receiving a first reset signal (see Fig. 4, timer 43 output) from the watchdog timer, and a reset circuit for generating a second reset signal (see Fig. 4, Fall Detecting Circuit 44 output) to be output to a predetermined circuit (see Fig. 4, flip-flop 45) of the microcomputer in response to the first reset signal; and

a watchdog timer (see Fig. 4, timer 43),

wherein the watchdog timer outputs the first reset signal to the microcomputer (see Column 3, Line 19).

Response to Arguments

Applicant's arguments filed 10/23/2007 have been fully considered but they are not deemed to be persuasive.

Regarding the 35 U.S.C. §101, problems, Applicant's response, amendment, and/or cancellations has overcome these rejections.

Regarding the 35 U.S.C. §112, second paragraph problems, Applicant's response, amendment, and/or cancellations has overcome these rejections.

Applicant Argues, claim 21 is not anticipated by Wakasugi. Wakasugi does not disclose, suggest, or motivate preventing the operation mode of a circuit being changed.

Examiner disagrees with applicant. The operation mode recited in claim 21 is very broad. As claimed, the operation mode can be 'initial program loading' and Wakasugi does disclose preventing that particular operation to take place (see Column 1, Lines 40-42).

Applicant's Arguments regarding claims 1-3, 6-9, and 11 are moot in view of new ground of rejection.

Allowable Subject Matter

The following is a statement of reasons for the indication of allowable subject matter, the prior art does not teach or fairly suggest in claims 13 and 16:

Claim 13 recites - a second control circuit for latching a fifth output signal from the control signal generator in response to a fourth output signal from the control signal generator, and for generating a second control signal responsive to a logical value of the fifth output signal latched in the second control circuit; and an OR gate for OR gating the first control signal and the second control signal and outputting an OR gate output as an operation mode setting signal.

Claim 16 recites - a second control circuit for latching a fifth output signal from the control signal generator in response to a fourth output signal from the control signal generator, and for generating a second control signal responsive to the logical value of the latched fifth output signal, and an OR gate for OR gating the first control signal and the second control signal and outputting an OR gate output as an operation mode setting signal.

Claims 4, 5,10, 14 and 15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 13 and 16 are objected to having formality problems, but would be allowable with appropriate corrections.

Conclusion

The prior arts made of record and not relied upon are considered pertinent to applicant's disclosure:

Bagley (U.S. Patent 5,655,083) discloses programmable reset system method for computer network;

Bergum et al. (U.S. Patent 5,249,227) discloses method and apparatus of controlling processing devices during power transition;

Hogan et al. (U.S. Patent 4,072,852) discloses digital computer monitoring and restart circuit;

Sibigtroth (U.S. Patent 4,580,246) discloses write protection circuit and method for a control register;

Nishitani (U.S. Patent 4,670,676) discloses reset and reset inhibit circuit; and

Bock et al. (U.S. Patent 5,155,856) discloses arrangement in a self-guarding data processing system for system initialization and reset.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hyun Nam whose telephone number is (571) 270-1725. The examiner can normally be reached on Monday through Friday 8:30 AM to 5:00 PM EST. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dr. Henry Tsai can be reached on (571) 272-4176. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

HENRY TSAI
SUPERVISORY PATENT EXAMINER

1/7/08